Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A non-volatile semiconductor memory ~~device comprising:~~ device, comprising:

a memory cell array including a plurality of bit lines and a plurality of memory cells arranged in a column direction and a row direction, wherein:

each of the memory cells has a source region, a drain region, a channel region disposed between the source region and the drain region, a word gate disposed to face the channel region, and a non-volatile memory element provided between the word gate and the channel region; ~~and~~

a voltage is respectively applied to the word gate, source region and drain region, when data is to be erased, read from or written to each of the plurality of memory cells;

a longitudinal section of the word gate has a base, a side which is perpendicular to the base, and a curved side which connects the base to the side;

each of the plurality of memory cells has a word gate support section that is disposed on an upper layer of the drain region;

a longitudinal section of the word gate support section has a base, a side that is perpendicular to the base, and a curved side that connects the base to the side;

the side of the word gate support section faces the side of the word gate;

the plurality of bit lines are respectively connected to the drain regions of the plurality of memory cells in each column that is arranged in the column direction; and

the word gate support section is formed of an insulator.

2-6. (Canceled)

7. (Currently Amended) The non-volatile semiconductor memory device as defined in ~~claim 2,~~

~~wherein~~ claim 1, the non-volatile memory element ~~is~~ being formed to extend between the word gate and the word gate support section.

8. (Canceled)

9. (Currently Amended) The non-volatile semiconductor memory device as defined in claim 1,

~~wherein~~ the non-volatile memory element ~~is~~ being formed of an ONO film which includes two oxide films (O) and a nitride film (N) between the two oxide films (O).

10. (Withdrawn) A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming a base material layer on a semiconductor layer and patterning the base material layer;

forming a trap layer on the entire surface of the semiconductor layer on which the base material layer is formed;

forming a first conductive layer on the trap layer, and shaping the first conductive layer into a plurality of sidewalls respectively provided on the sides of the patterned base material layer with the trap layer interposed;

forming a first insulating film which covers the sidewalls of the first conductive layer and the base material layer;

forming a second conductive layer which is in contact with the semiconductor layer between adjacent two of the sidewalls of the first conductive layer; and

shaping the base material layer into a plurality of sidewalls.

11. (Withdrawn) The method of manufacturing a non-volatile semiconductor memory device as defined in claim 10,

wherein the base material layer is an insulating layer.

12. (Withdrawn) The method of manufacturing a non-volatile semiconductor memory device as defined in claim 10,

wherein the base material layer is a conductive layer.

13. (Withdrawn) A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming a two-layer structure including a trap layer disposed on a semiconductor layer and a first conductive layer formed on the trap layer;

forming a plurality of word gate support sections each having a shape of sidewall respectively on the sides of the two-layer structure;

forming a second conductive layer which is in contact with the semiconductor layer between adjacent two of the word gate support sections;

shaping the first conductive layer into a plurality of word gate layers each having a shape of sidewall; and

etching part of the trap layer between adjacent two of the word gate layers.

14. (Withdrawn) A method of manufacturing a non-volatile semiconductor memory device, comprising:

forming a first conductive layer which is in contact with a diffusion region in a semiconductor layer;

forming a trap layer on the entire surface of the semiconductor layer on which the first conductive layer is formed;

forming a second conductive layer on the trap layer;

shaping the second conductive layer into a plurality of sidewalls respectively provided on the sides of the first conductive layer; and

etching part of the trap layer between adjacent two of sidewalls of the second conductive layer.

15. (New) A non-volatile semiconductor memory device, comprising:

a memory cell array including a plurality of bit lines and a plurality of memory cells arranged in a column direction and a row direction, wherein:

each of the memory cells has a source region, a drain region, a channel region disposed between the source region and the drain region, a word gate disposed to face the channel region, and a non-volatile memory element provided between the word gate and the channel region;

a voltage is respectively applied to the word gate, source region and drain region, when data is to be erased, read from or written to each of the plurality of memory cells;

a longitudinal section of the word gate has a base, a side that is perpendicular to the base, and a curved side that connects the base to the side;

each of the plurality of memory cells has a word gate support section that is disposed on an upper layer of the source region;

a longitudinal section of the word gate support section has a base, a side that is perpendicular to the base, and a curved side that connects the base to the side;

the side of the word gate support section faces the side of the word gate;

the plurality of bit lines are respectively connected to the source regions of the plurality of memory cells in each column that is arranged in the column direction; and

the word gate support section is formed of an insulator.

16. (New) The non-volatile semiconductor memory device as defined in claim 15, the non-volatile memory element being formed to extend between the word gate and the word gate support section.

17. (New) The non-volatile semiconductor memory device as defined in claim 15, the non-volatile memory element being formed of an ONO film that includes two oxide films (O) and a nitride film (N) between the two oxide films (O).